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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ozis et al.
Application No. 10/683,575
Filed: October 9, 2003
Confirmation No. 9457
For: MODELING SUBSTRATE NOISE COUPLING USING SCALABLE PARAMETERS
Examiner: --
Art Unit: 2123
Attorney Reference No. 245-66956-01

CERTIFICATE OF MAILING

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Attorney for Applicants

Date Mailed 9/3/04

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97(b)(3)

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Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

If the present application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55). Applicants will provide copies of such patents upon request.

Applicants filed this Information Disclosure Statement ("IDS") before the mailing date of a first Office action on the merits. As a result, no fee should be required to file this IDS.

However, if the Patent Office determines that a fee is required for Applicants to file this IDS, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550. A **duplicate** copy of this Information Disclosure Statement is enclosed.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

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Filing Date	October 9, 2003
First Named Inventor	Ozis
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Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Blalack et al., "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate," *IEEE IEDM 96*, pp. 623-626 (1996).
		Blalack, "Switching Noise in Mixed-Signal Integrated Circuits," Department of Electrical Engineering, Stanford University, 3 pp. from http://cis.stanford.edu/icl/wooley-grp/tallis/tallis.html (accessed on February 18, 2004).
		Blalack et al., "The Effects of Switching Noise on an Oversampling A/D Converter," *1995 IEEE International Solid-State Circuits Conference*, pp. 200-201, 367 (1995).
		Charbon et al., "Substrate Optimization Based on Semi-Analytical Techniques," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 2, pp. 172-190 (February 1999).
		Costa et al., "Efficient Techniques for Accurate Modeling and Simulation of Substrate Coupling in Mixed-Signal IC's," *IEEE Trans. Computer-Aided Design*, Vol. 18, No. 5, pp. 597-607 (May 1999).
		Gharpurey et al., "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE 1995 Custom Integrated Circuits Conference*, pp. 125-128 (1995).
		Gharpurey et al., "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, pp. 344-353 (March 1996).
		Hewlett Packard, "S-Parameter Techniques for Faster, More Accurate Network Design," Test & Measurement Application Note 95-1 (1997).
		Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 10, pp. 1212-1219 (October 1994).
		Johnson et al., "Chip Substrate Resistance Modeling Technique for Integrated Circuit Design," *IEEE Transactions on Computer-Aided Design*, Vol. CAD-3, No. 2, pp. 126-134 (April 1984).
		Kwan et al., "Simulation and Analysis of Substrate Coupling in Realistically-Large Mixed-A/D Circuits," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 184-185 (1996).
		Merrill et al., "Effect of Substrate Material on Crosstalk in Mixed Analog/Digital Integrated Circuits," *IEEE IEDM 94*, pp. 433-436 (1994).
		Mitra et al., "A Methodology for Rapid Estimation of Substrate-Coupled Switching Noise," *IEEE 1995 Custom Integrated Circuits Conference*, pp. 129-132 (1995).

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* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		Özişş, Dicle "An Efficient Modeling Approach for Substrate Noise Coupling Analysis with Multiple Contacts in Heavily Doped CMOS Processes," Masters Thesis, Oregon State University, OR, 93 pp. (2002).
		Özişş, et al., "A Comprehensive Geometry-Dependent Macromodel for Substrate Noise Coupling in Heavily Doped CMOS Processes," *IEEE 2002 Custom Integrated Circuits Conference*, pp. 497-500 (2002).
		Özişş, et al., "An Efficient Modeling Approach for Substrate Noise Coupling Analysis," *IEEE ISAS*, pp. 237-240 (May 2002).
		Pfost et al., "Modeling Substrate Effects in the Design of High-Speed Si-Bipolar IC's," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 10, pp. 1493-1501 (October 1996).
		Pun et al., "Experimental Results and Simulation of Substrate Noise Coupling via Planar Spiral Inductor in RF ICs," *IEEE IEDM 97*, pp. 325-328 (1997).
		Raskin et al., "Coupling Effects in High-Resistivity Simox Substrates for VHF and Microwave Applications," *Proceedings 1995 IEEE International SOI Conference*, pp. 62-63 (October 1995).
		Raskin et al., "Substrate Crosstalk Reduction Using SOI Technology," *IEEE Transactions on Electron Devices*, Vol. 44, No. 12, pp. 2252-2261 (December 1997).
		Sadate, "A Substrate Noise Coupling Model for Lightly Doped CMOS Processes," Masters Thesis, Oregon State University, OR, 56 pp. (2001).
		Samavedam et al., "A Scalable Substrate Noise Coupling Model for Mixed-Signal ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 128-131 (1999).
		Silveira et al., "Efficient Reduced-Order Modeling of Frequency-Dependent Coupling Inductances Associated with 3-D Interconnect Structures," *IEEE/ACM Proc. DAC*, pp. 376-380 (June 1995).
		Smedes et al., "Boundary Element Methods for 3D Capacitance and Substrate Resistance Calculations in Inhomogeneous Media in a VLSI Layout Verification Package," *Advances in Engineering Software*, Vol. 20, No. 1, pp. 19-27 (1994).
		Smedes et al., "Layout Extraction of 3D Models for Interconnect and Substrate Parasitics," *ESSDERC'95 25th European Solid State Device Research Conference*, 4 pp. (September 1995).
		Stanisic et al., "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 3, pp. 226-238 (March 1994).

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		Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 420-430 (April 1993).
		van Genderen et al., "Modeling Substrate Coupling Effects using a Layout-to-Circuit Extraction Program," *Proceedings of the ProRISC Workshop on Circuits, Systems, and Signal Processing*, pp. 173-178 (1997).
		Verghese et al., "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 3, pp. 314-323 (March 1998).
		Verghese et al., "Fast Parasitic Extraction for Substrate Coupling in Mixed-Signal ICs," *IEEE 1995 Custom Integrated Circuits Conference*, pp. 121-124 (1995).
		Verghese et al., "Verification Techniques for Substrate Coupling and Their Application to Mixed-Signal IC Design," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, pp. 354-365 (March 1996).
		Viviani et al., "Extended Study of Crosstalk in SOI-SIMOX Substrates," *IEEE IEDM 95*, pp. 713-716 (1995).
		Wemple et al., "Mixed-Signal Switching Noise Analysis Using Voronoi-Tessellated Substrate Macromodels," *32nd Design Automation Conference*, 6 pp. (1995).

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